REMARKS/ARGUMENTS

Favorable reconsideration of this application as presently amended and in light of the following discussion is respectfully requested.

Claims 1-21 are currently pending in this case, Claims 1 and 9 have been amended, and Claim 21 has been added by the present Amendment. No new matter has been added.

In the outstanding Official Action, the drawings are objected to; Claims 1-9 and 11-20 are rejected under 35 U.S.C. 102(e) as being anticipated Japanese Pat. No. 11-45125 (hereinafter JP'125); Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over JP'125 in view of U.S. Patent No. 6,133,719 to Maulik (hereinafter "Maulik").

Applicant noticed that the 102(e) rejection is improper, because the cited reference is a Japanese patent, not an US patent or an US published application. In a phone interview with the Examiner, it was clarified that the citation of 102(e) was a typographic error, and the rejection is either 102(a) or 102(b). Therefore the present amendment proceeds to discuss the patentability of the claims on the merits.

In response to the objection to the drawings, Figures 17, 18, and 19 have been labeled as "Prior Art". Applicant respectfully submits the objection to the drawings has been overcome.

Claim 18 recites to a reference power supply circuit comprising a first PN junction, a second PN junction, a first resistive element, a current supply, and a mirror circuit. New Claim 21, depending on Claim 18, further recites elements included in the mirror circuit and how these elements are connected within the circuit structure. Claim 21 is supported by the originally filed specification.[1]

Briefly recapitulating, Claim 1 is directed to a reference power supply circuit comprising a first PN junction, a first PN junction, a first current supply, a first resistive

[1] Specification, Figure 16, and from page 24, line 9 to page 26, line 6.

element, a second resistive element, a second current supply, a third current supply, and a differential amplifier. Claim 1 is amended to further specify that "**the first current supply [is] supplying a current only to the first PN junction.**" Support for the amendment to Claim 1 is found in the originally filed specification and Figures 1, 12, 13, 14, and 15. The circuit with the structural features recited in Claim 1 has stable temperature characteristics, as long as the size ratio between the first PN junction and the second PN junction is maintained.[2] Therefore, the sizes of the first PN junction and the second PN junction can be set to be half of those in JP'125. A person of ordinary skill in the art can not derive such a significant advantage based on the teachings from JP'125.

The reference voltage generating circuit disclosed by JP'125, contains a resistive element R4 connected in parallel with the diode D1 (Figures 12 and 20). Therefore, the current source P1 supplies current to both the diode D1 and the resistive element R4. JP'125 does not teach the positively recited feature of amended Claim 1, that "the first current supply [supplies] a current only to the first PN junction." Because JP'125 does not disclose or suggest all the elements of independent Claim 1, Applicant respectfully submits that Claim 1 and all claims depending therefrom, are not anticipated by the asserted prior art for at least the reasons stated above.[3]

Claim 9 recites a reference power supply circuit comprising a first diode, a second diode, a first transistor, a first resistive element, a second resistive element, a second transistor, a third transistor and a differential amplifier. Claim 9 is amended to clarify that "**the first transistor [is] supplying a current only to the first diode.**" Support for the amendment is found in the originally filed specification and Figures 6, 8, 9, and 10. As

[2] See in Specification from page 13, line 26, to page 15, line 26.
[3] MPEP § 2142 "...the prior art reference (or references when combined) must teach or suggest **all** the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991)."

discussed relative to Claim 1, because the first diode does not have a resistive element connected in parallel, the temperature characteristics are stable as long as the size ratio between the first diode and second diode is maintained. The sizes of the first diode and second diode can be set to be half those in JP'125A, which constitutes a significant advantage that a person of ordinary skill in the art could not infer from on the teachings from JP'125 .

JP'125 does not teach or suggest the feature recited in Claim 9, that all the current supplied by the first transistor (acting as a current source) flows only through the first diode. The reference voltage generating circuit disclosed by JP'125, includes a resistive element R4 in parallel with the diode D1 (Figures 12 and 20). Therefore, the current is supplied to both the diode D1 and the resistive element R4. Because JP'125 does not teach or suggest all the elements of independent Claim 9, it is respectfully submitted that amended Claim 9 and all the claims depending therefrom, are patentably defined over the cited reference.

The reference power supply circuit recited in Claim 18 includes a mirror circuit, which copies the current flowing through the first PN junction, to the first, the second resistive elements and the second PN junction, and also controls the current supply in accordance with the current flowing through the first, the second resistive elements and second PN junction. An advantage of the circuit recited in Claim 18 is that unlike a differential amplifier, the mirror circuit does not have a voltage gain and thus, it is not necessary to consider how to prevent oscillation.

In Figure 20 from JP'125, the mirror circuit including the NMOS transistors N20 and N21 generates a reference current I_{ref}, and is connected via a PMOS transistor P3 to the potential VDD. The mirror current circuit in JP'125 is not linked to any of the diodes (see D1, D2), so it can not perform the functionality recited for the mirror circuit in Claim 18. The mirror circuit in JP'125 has different position within the structure and different

functionality than the mirror circuit recited in Claim 18. Therefore, Applicant respectfully submits that Claim 18 and all claims depending therefrom, are not anticipated by the asserted prior art.

Accordingly, in view of the present amendment no further issues are believed to be outstanding and the present application is believed to be in condition for formal allowance. An early and favorable action to that effect is respectfully requested.

Respectfully submitted,

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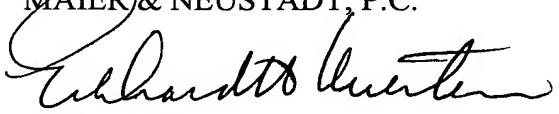
MAIER & NEUSTADT, P.C.



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IN THE DRAWINGS

The attached sheet of drawings includes changes to Fig. 17, 18 and 19. The figures have been labeled as "Prior Art". The sheets, which includes Fig. 17, 18, and 19, replace the original sheets including Fig. 17, 18, and 19.

Attachment: Replacement Sheets